## Lab 3

## Môn: Hệ thống số (TN)

## Lớp: L01

## Nhóm: 7

## GVHD: Kiều Đỗ Nguyên Bình

## Thành viên: Lê Đức Huy 1810166

## Nguyễn Gia Huy 1810173

## Huỳnh Thiên Trình 1810615

## Lê Bá Thông 1810555

## Lê Duy Bình 51204735

1. **Introduction**
   1. **Aims**
      * Implement half adder, full adder circuit.
      * Practice with different adder circuits.

## Requirements

* + - Understand how to implement an adder circuit.
    - Have ability to combine the small cicuits to implement the bigger ones.

## Procedure

* + - Verify the gates.
    - Make the connections as per the circuit diagram.
    - Switch on *Vcc* and apply various combinations of input according to the truth table.
    - Note down the output readings for half/full adder and half/full subtractor sum/difference and the carry/borrow bit for different combinations of inputs.

## Report Requirements

Your report of each exercise should include:

* + - Answer and explain all questions (If required).
    - The circuit and truth table of each exercise.
    - Two or Three photos of the circuit **on KIT**.

# Contents

## Half/Full Adder

### Using X-OR and Basic Gates Half Adder

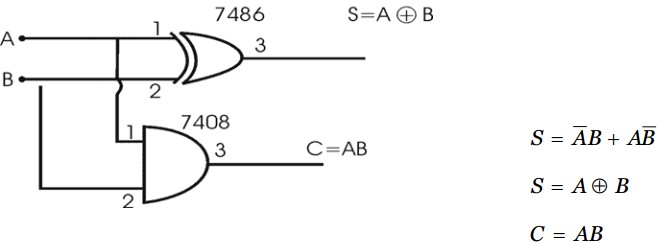


Figure 1: Half Adder circuit with X-OR and Basic Gates.

### Full Adder

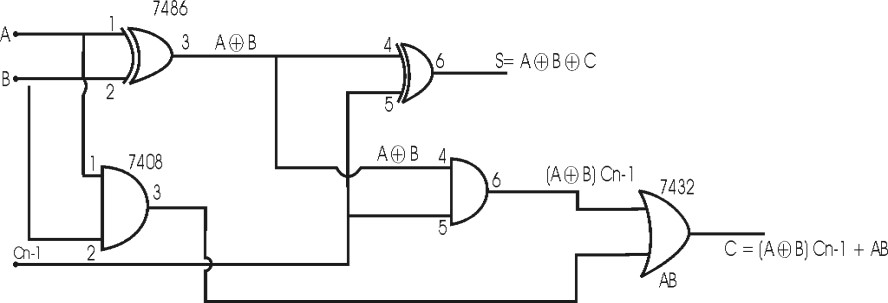


Figure 2: Full Adder circuit with X-OR and Basic Gates.

### Using only NAND gates Half Adder

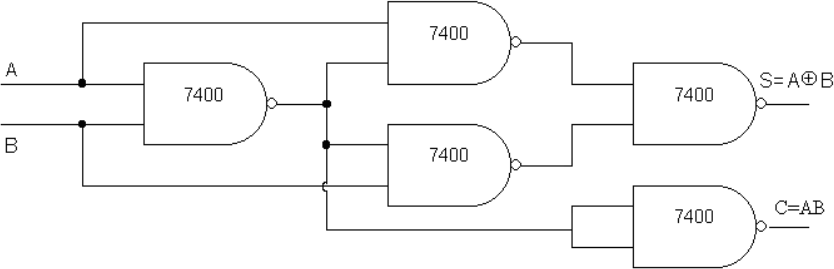


Figure 3: Half Adder circuit with only NAND gates.

### Full Adder

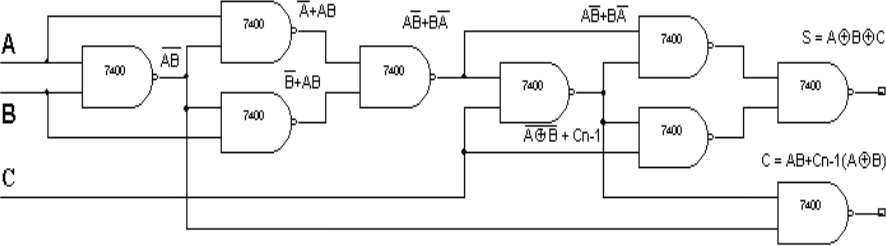


Figure 4: Full Adder circuit with only NAND gates.

## Half/Full Subtractor

### Using X-OR and Basic Gates Half Subtractor

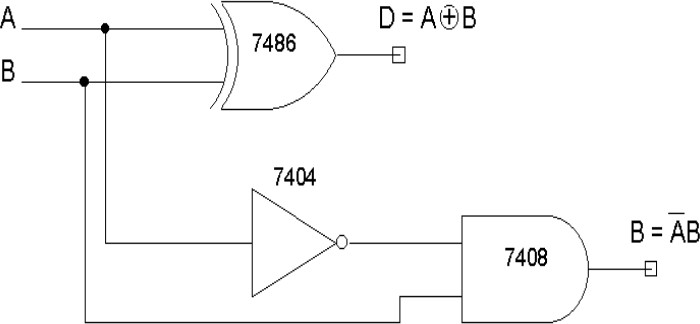


Figure 5: Half Subtractor circuit with X-OR and Basic Gates.

### Full Subtractor

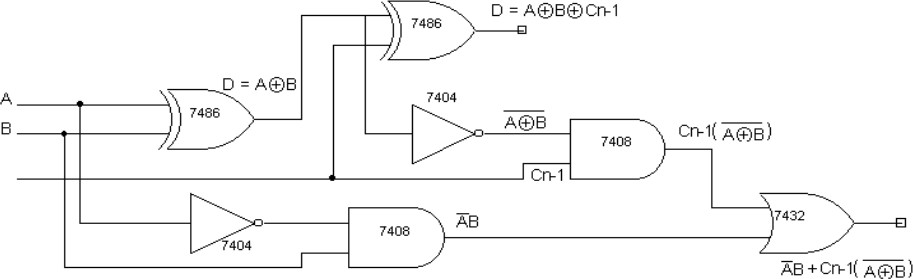


Figure 6: Full Subtractor circuit with X-OR and Basic Gates.

### Using only NAND gates Half Subtractor

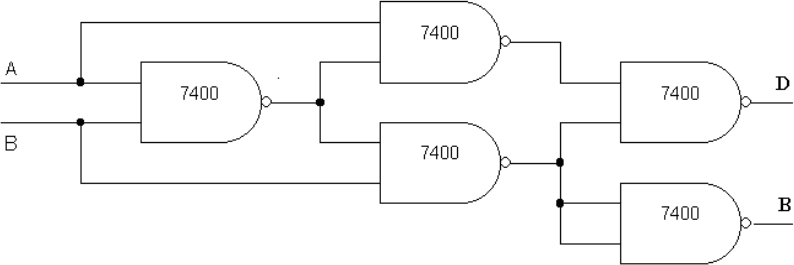


Figure 7: Half Subtractor circuit with only NAND gates.

### Full Subtractor

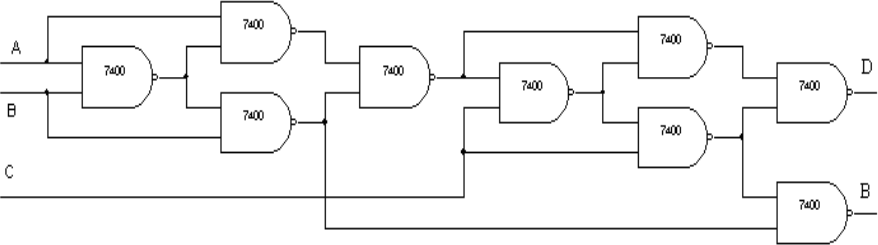


Figure 8: Full Subtractor circuit with only NAND gates.

### Fill in these tables:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Half Adder** | | | | | |
| **A** | **B** | **S** | **C** | **S(V)** | **C(V)** |
| **0** | **0** | **0** | **0** | **0** | **0** |
| **0** | **1** | **1** | **0** | **1** | **0** |
| **1** | **0** | **1** | **0** | **1** | **0** |
| **1** | **1** | **0** | **1** | **0** | **1** |

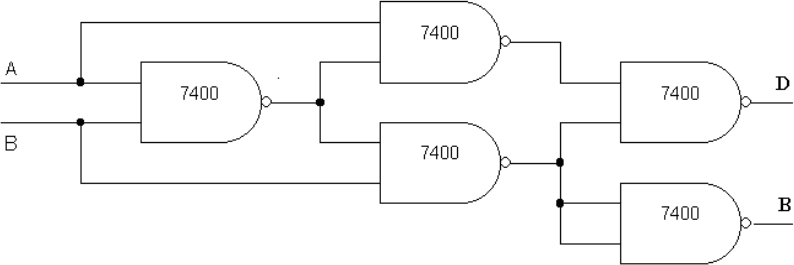
|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Half Subtractor** | | | | | |
| **A** | **B** | **D** | **B** | **D(V)** | **B(V)** |
| **0** | **0** | **0** | **0** | **0** | **0** |
| **0** | **1** | **1** | **1** | **1** | **1** |
| **1** | **0** | **1** | **0** | **1** | **0** |
| **1** | **1** | **0** | **0** | **0** | **0** |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Full Adder** | | | | | | |
| **A** | **B** | **Cn-1** | **S** | **C** | **S(V)** | **C(V)** |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **0** | **0** | **1** | **1** | **0** | **1** | **0** |
| **0** | **1** | **0** | **1** | **0** | **1** | **0** |
| **0** | **1** | **1** | **0** | **1** | **0** | **1** |
| **1** | **0** | **0** | **1** | **0** | **1** | **0** |
| **1** | **0** | **1** | **0** | **1** | **0** | **1** |
| **1** | **1** | **0** | **0** | **1** | **0** | **1** |
| **1** | **1** | **1** | **1** | **1** | **1** | **1** |

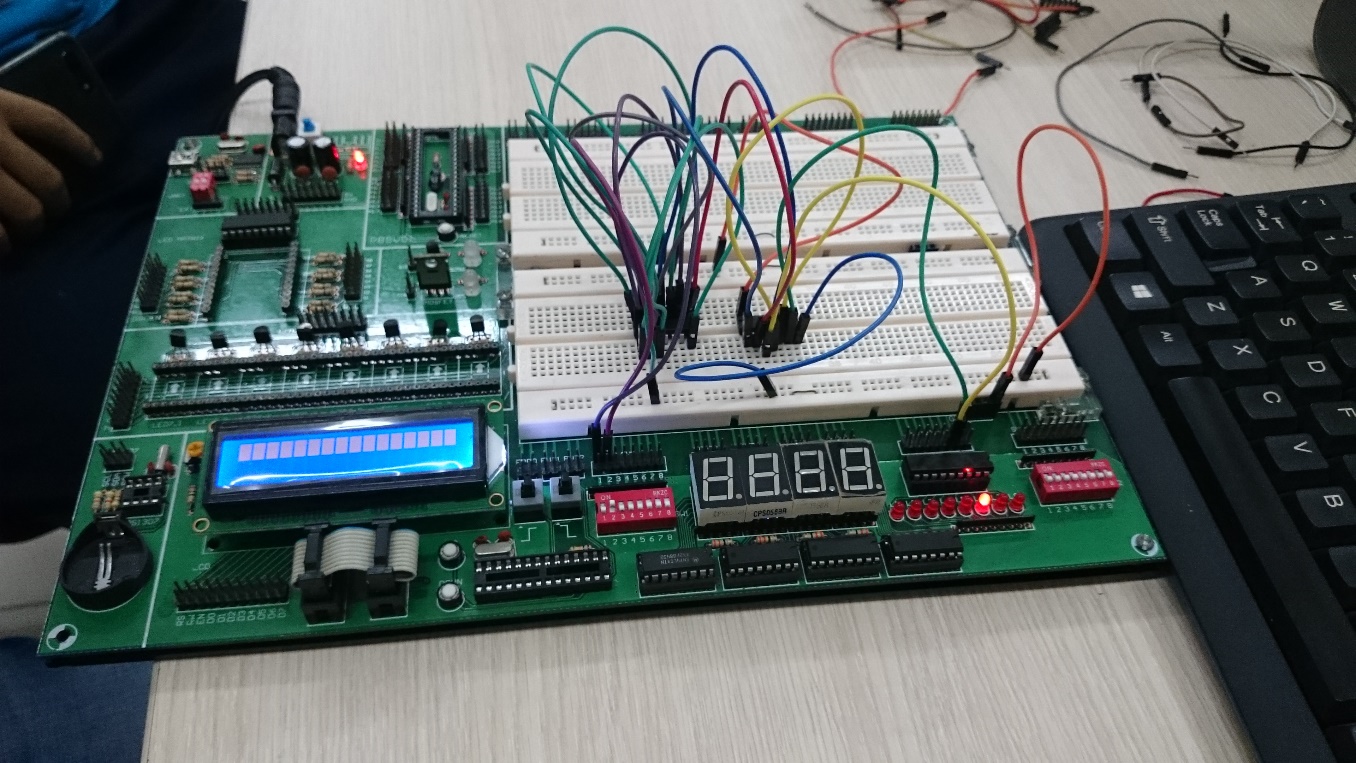
|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Full Subtractor** | | | | | | |
| **A** | **B** | **Cn-1** | **D** | **B** | **D(V)** | **B(V)** |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **0** | **0** | **1** | **1** | **1** | **1** | **1** |
| **0** | **1** | **0** | **1** | **1** | **1** | **1** |
| **0** | **1** | **1** | **0** | **1** | **0** | **1** |
| **1** | **0** | **0** | **1** | **0** | **1** | **0** |
| **1** | **0** | **1** | **0** | **0** | **0** | **0** |
| **1** | **1** | **0** | **0** | **0** | **0** | **0** |
| **1** | **1** | **1** | **1** | **1** | **1** | **1** |

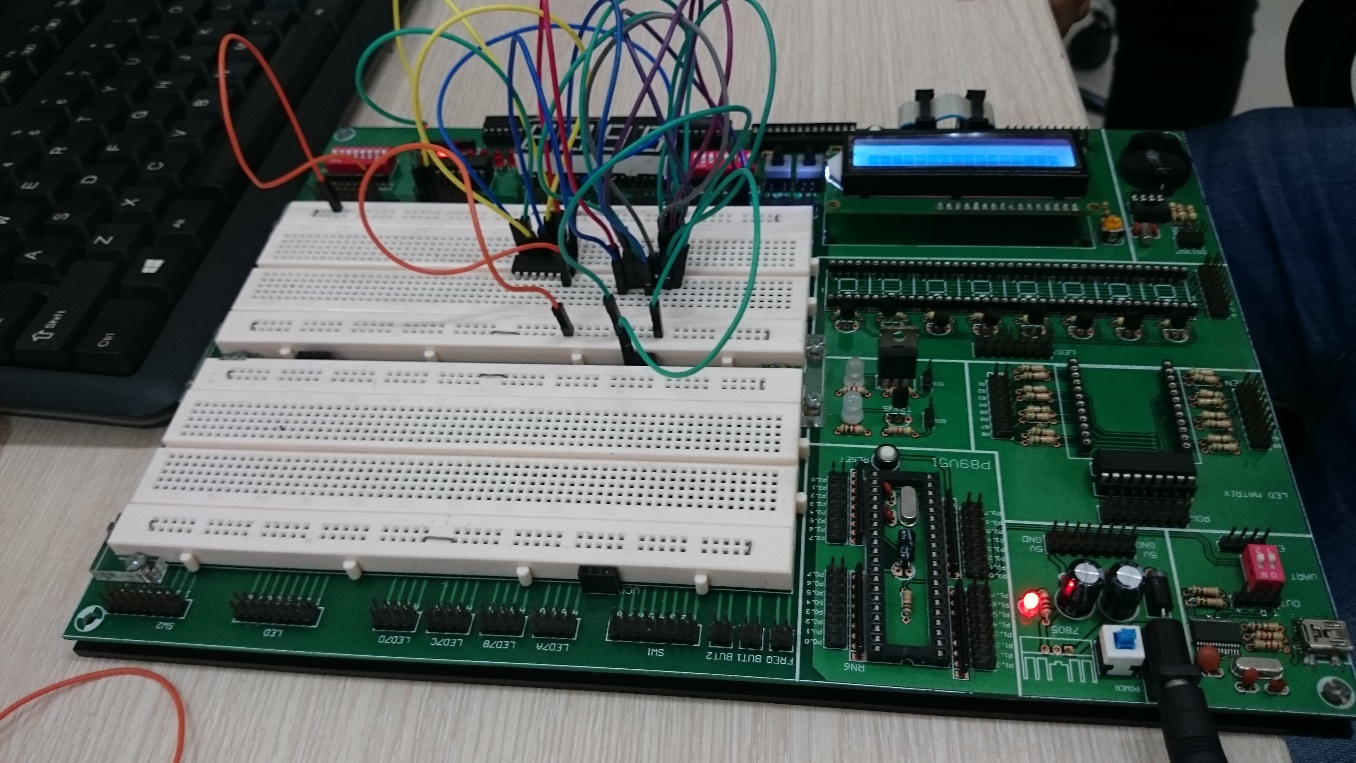
1. **Exercices**

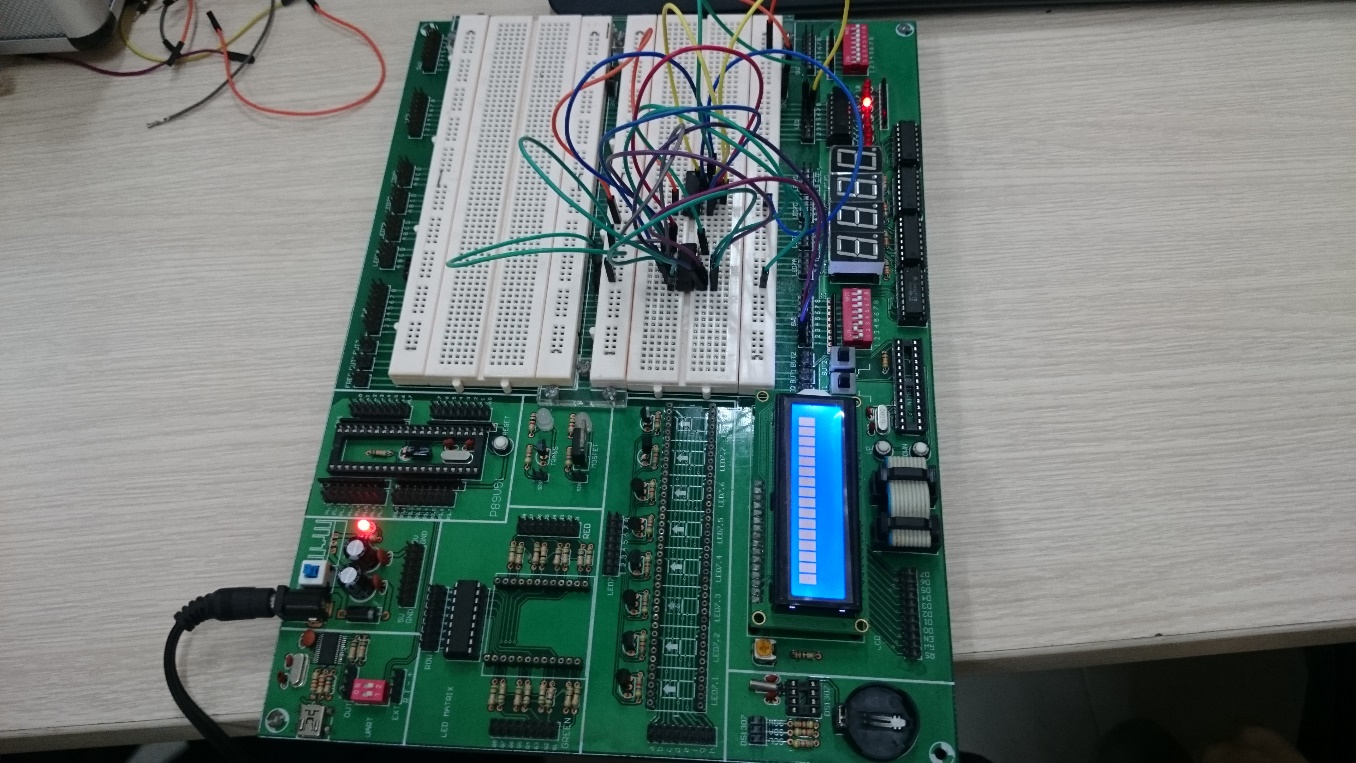
**Exercice 1**: Implement a half subtractor circuit use **only** NAND gate. Show results on LED diode.



|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Half Subtractor** | | | | | |
| **A** | **B** | **D** | **B** | **D(V)** | **B(V)** |
| **0** | **0** | **0** | **0** | **0** | **0** |
| **0** | **1** | **1** | **1** | **1** | **1** |
| **1** | **0** | **1** | **0** | **1** | **0** |
| **1** | **1** | **0** | **0** | **0** | **0** |

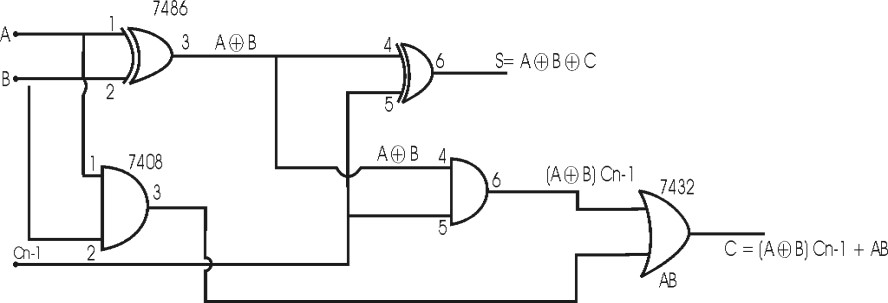




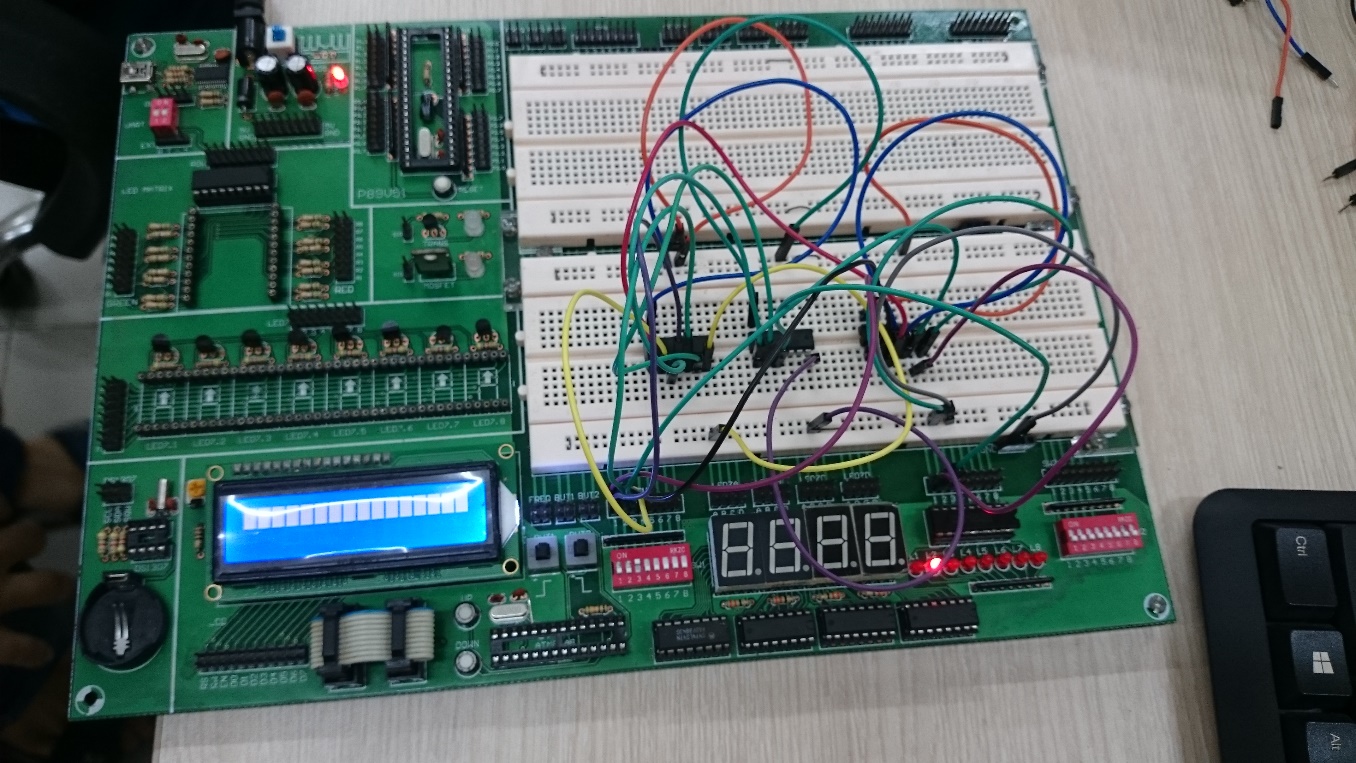


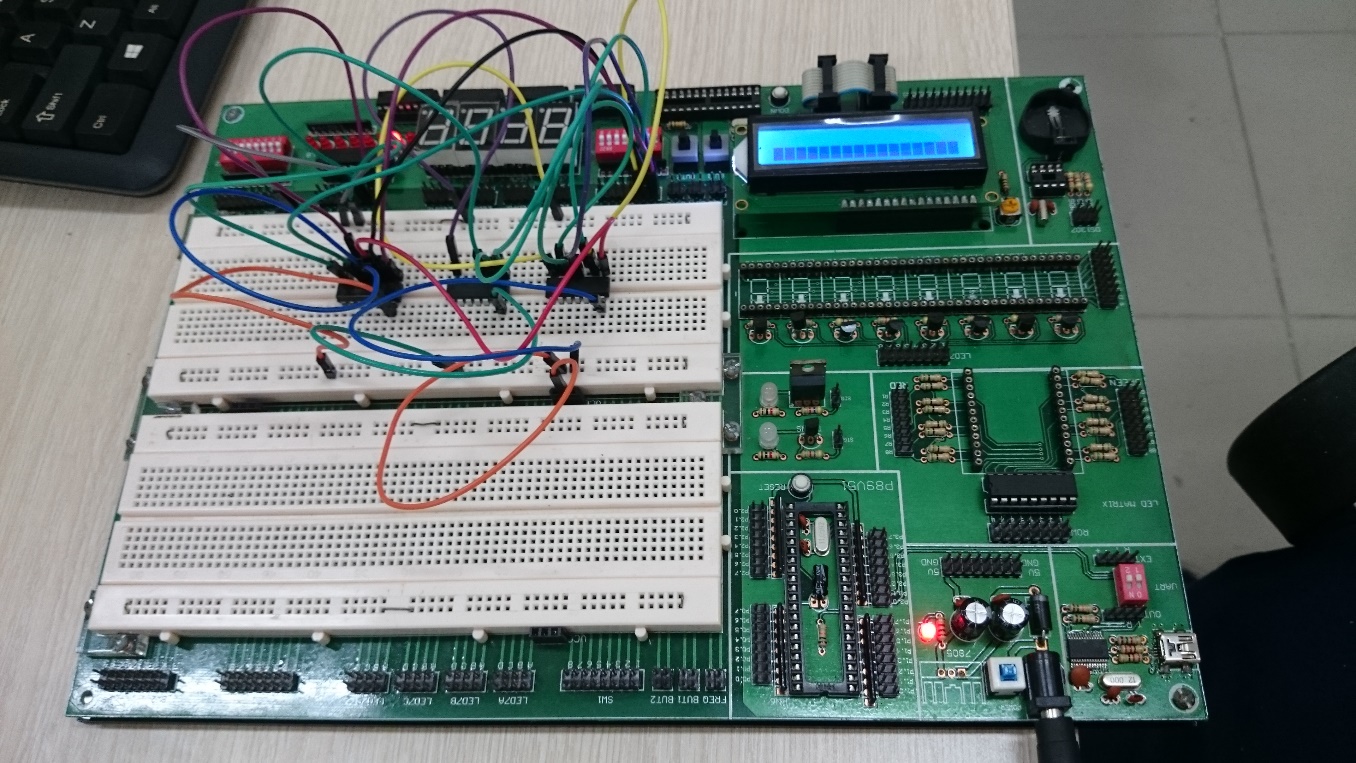
**Exercice 2**: Implement full adder circuit **from the half adder**

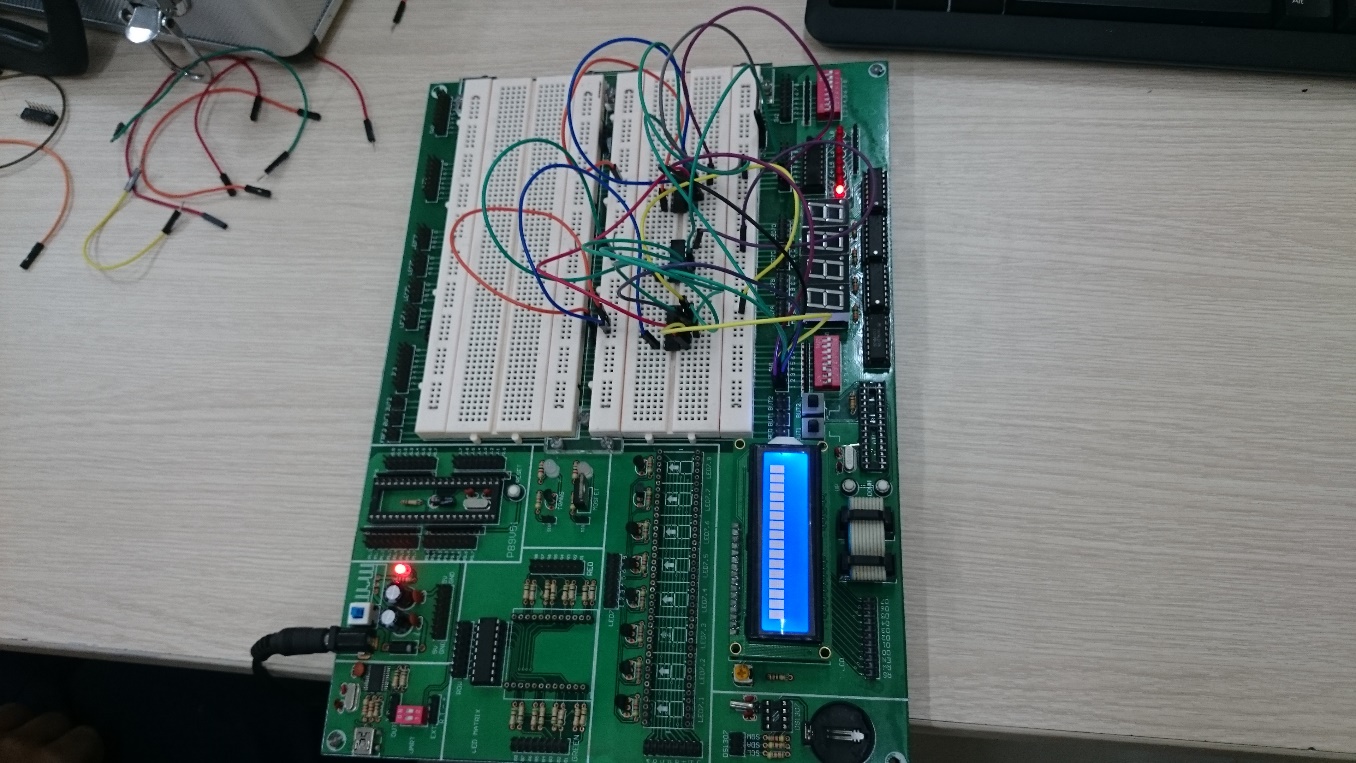
The full adder circuit must have 3 inputs: bit A, bit B and carry bit. Show results on LED diode.

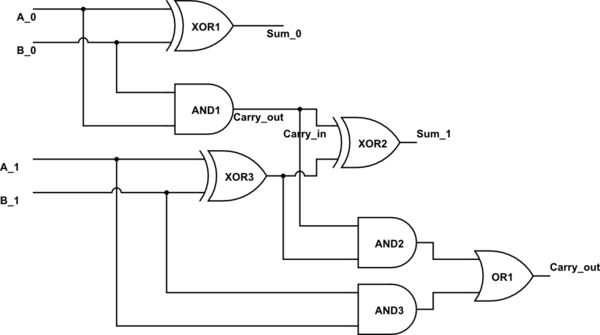


|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Full Adder** | | | | | | |
| **A** | **B** | **Cn-1** | **S** | **C** | **S(V)** | **C(V)** |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **0** | **0** | **1** | **1** | **0** | **1** | **0** |
| **0** | **1** | **0** | **1** | **0** | **1** | **0** |
| **0** | **1** | **1** | **0** | **1** | **0** | **1** |
| **1** | **0** | **0** | **1** | **0** | **1** | **0** |
| **1** | **0** | **1** | **0** | **1** | **0** | **1** |
| **1** | **1** | **0** | **0** | **1** | **0** | **1** |
| **1** | **1** | **1** | **1** | **1** | **1** | **1** |







**Exercice 3**: Implement an adder that can be work out the sum of two 2-bits numbers by using full adder circuit. Show results on both LED diot and 7-seg LED.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Inputs** | | | | **Outputs** | | | |
| **a1** | **a0** | **b1** | **b0** | | **c1** | **s1** | **s0** |
| **0** | **0** | **0** | **0** | | **0** | **0** | **0** |
| **0** | **0** | **0** | **1** | | **0** | **0** | **1** |
| **0** | **0** | **1** | **0** | | **0** | **1** | **0** |
| **0** | **0** | **1** | **1** | | **0** | **1** | **1** |
| **0** | **1** | **0** | **0** | | **0** | **0** | **1** |
| **0** | **1** | **0** | **1** | | **0** | **1** | **0** |
| **0** | **1** | **1** | **0** | | **0** | **1** | **1** |
| **0** | **1** | **1** | **1** | | **1** | **0** | **0** |
| **1** | **0** | **0** | **0** | | **0** | **1** | **0** |
| **1** | **0** | **0** | **1** | | **0** | **1** | **1** |
| **1** | **0** | **1** | **0** | | **1** | **0** | **0** |
| **1** | **0** | **1** | **1** | | **1** | **0** | **1** |
| **1** | **1** | **0** | **0** | | **0** | **1** | **1** |
| **1** | **1** | **0** | **1** | | **1** | **0** | **0** |
| **1** | **1** | **1** | **0** | | **1** | **0** | **1** |
| **1** | **1** | **1** | **1** | | **1** | **1** | **0** |

